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Performance Enhancement of DVR for Mitigating Voltage Sag/Swell using Vector Control Strategy

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Abstract

This paper presents dynamic voltage restorer (DVR) with vector control strategy for mitigating power quality in power distribution systems. Whenever power quality problems, voltage sag/swell, occur DVR has to automatically detect and inject voltage components. The detection unit should be fast enough to know the variation of all phase voltages, including magnitude and phase, to trigger the DVR to inject appropriate voltage components with required phase angles within very short period of time. Here, control strategy adopted for driving the DVR plays and important role in its performance. Any delay in the process or incorrect injection would be harmful to sensitive loads that are vulnerable to voltage sag/swell. This paper illustrates vector control strategy based on decoupling control to enhance performance of DVR during the process of compensation. It was found out that voltage sags/swells can be corrected faster with the proposed control strategy compared to conventional methods.

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Keywords: Dynamic voltage restorer; vector control algorithm; voltage sag; voltage swell.

1. Introduction

Industrial and commercial consumers of electrical power are becoming increasingly sensitive to power quality problems. When disruptions occur in consumers' premises due to poor power quality, downtime, defects and loss of production, and damage to equipment can be substantial. This would result in financial losses to consumers as well as utilities. Hence, the study of electrical power quality is becoming a popular

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research topic. One of the power quality problems that are typical in all distribution system is voltage sag/swell. The voltage sags/swells are caused by remote faults or switching of large loads (e.g. motor starting and energize capacitor or transformer) [1]. Voltage sag is defined as a short duration reductions in

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Nomenclature

DVR	Dynamic voltage restorer
ASD	Adjustable speed drives
PLC	Programmable logic controllers
PCC	Point of common coupling
PI	Proportional-integral
VSC	Voltage source converter
PWM	Pulse width modulation unit
ESD	Energy storage device
DRU	Detection and reference generation unit
KCL	Kirchhoff's current law
PLL	Phase-Locked Loop

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the *rms* voltage that can last a few cycles, with reduction in voltage ranging from 0.9 to 0.1 p.u. of nominal voltage. Voltage swell, on the other hand, is defined as a short duration increasing in *rms* voltage with increase in voltage ranging from 1.1 to 1.8 p.u. of nominal voltage [2]. Through the voltage sags/swells last as little as a few cycles, they can disrupt some sensitive loads such as adjustable speed drives (ASD), programmable logic controllers (PLC), and semiconductor plants.

There are various solutions to this problem, such as designing inverter drives for process equipment to be more tolerant to voltage fluctuations or installation of voltage correction devices. It has been shown that for customers of large loads, from a high kVA to low MVA range, good solutions are installation of custom power device such as DVR [3]. Applications of DVR are mainly for protecting the sensitive loads that may be considerably affected by fluctuation in distribution voltage. Fig. 1 shows a single line diagram of power distribution system with DVR protecting a sensitive load. Assuming a short circuit fault occurs at A, the voltage at A will be dropped to 0 p.u. and the voltage at point B will also be reduced about 0.64 p.u. With this condition for sure any sensitive load that is vulnerable to voltage sag will be affected. In order to protect the sensitive or critical load, DVR is installed at point of common coupling (PCC). The voltage at this bus will be remaining at 1.0 p.u. due to the presence of DVR. It means that the main function of DVR has to maintain the amplitude and phase angle of load voltage. However, upon detecting a fault DVR should "react" quickly to correct the problem. A fast control strategy is desirable to increase the performance of DVR.
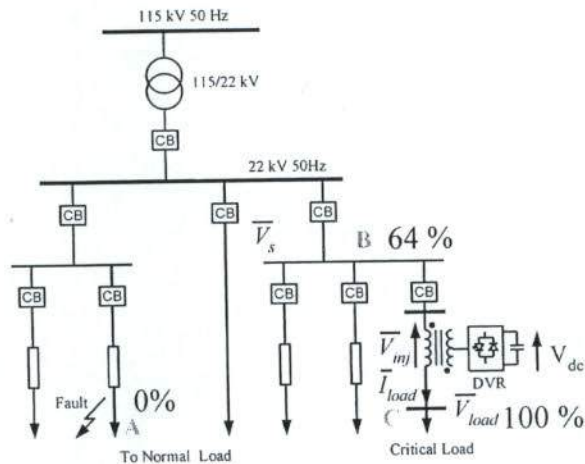
Fig. 1. Simplified diagram of DVR protecting a sensitive load.

The control strategy of DVR can be classified into two parts namely detection of voltage sag/swell and injection of the voltage component [4]-[10]. The Open loop control method as a conventional one is generally used for driving DVR because of its simplicity and low cost. However, there are several drawbacks such as the dependency on filter dynamics and sustained voltage oscillations in power system. Since the response time against voltage sags/swell varies according to the dynamics of inductance and capacitance of the ripple filter. The open loop with feedforward control can reduce the tracking time to deal with the unexpected voltage sag but still have the error on transient state. The double loop control can compensate the transient state error. But, the steady state load voltage may not be compensated to a desired value owing to voltage drop across the transformer series impedance and the filter. Therefore, it is required to compensate with regulation for the ripple filter current of the DVR circuit as an advanced control strategy for driving DVR.

The proportional-integral (PI) control scheme is commonly used in conventional control system due to simple algorithm and structure [6]–[8]. Consequently, the synchronous PI decoupling control scheme is adopted as control strategy for driving DVR against voltage disturbances. This control strategy is derived on the basis of the restoration of linearity in control performance using control variables such as inductor currents in the ripple filter and compensating voltages injected through transformer [10]. The coupling terms in circuit equations expressed in the synchronous reference frame, which deteriorate the linearity in control performance, will be easily removed by adding as feedforward terms. Therefore, the linearity can be retrieved so that it is easy to control dq control variables independently. This control scheme has the characteristics such as fast response without voltage oscillation in the transient state and low error in the steady state. The fast response in transient state guarantees faster action against the voltage sag/swell and the low error in steady state guarantees enough voltage compensation against voltage sag/swell. Moreover, since the currents flowing through the ripple filter inductor are used as the supplementary control variables, it is possible to regulate the inductor current within a permitted limit. Accordingly, the surge current flowing into the switching power device can be prevented thoroughly. Therefore, this paper proposes vector control strategy for improving dynamic performance of DVR. The controller design is based on state-space model and voltage vector control model. The voltage and current vector control is

used to produce the appropriate output components. The output filter is also used to compute the control parameters and theoretical considerations have been verified by simulation results.

This paper is organized as follows. The system configuration of DVR is presented in Section 2. Section 3 describes the DVR control strategies against voltage sag and swell. In Section 4, the mathematical model of DVR using synchronous reference frame is presented. The control design of DVR is elaborated in Section 5. Section 6 shows the simulation results for both balanced and unbalanced conditions. Finally, contributions and conclusions of the paper are summarized in Section 7.

2. System Configuration of DVR

Figure 2 shows components of DVR and their typical connection. The DVR consists of multi-level voltage source converter (VSC) [1], detection and reference generation unit (DRU), pulse width modulation unit (PWM), control unit, output filter, injection transformer, DC link and energy storage device (ESD). The measured voltage and currents are input signals to DRU. It gives signals to the control unit when the measured quantities differ from the settings of the controller. The DRU triggers start of compensation when the supply voltage comes outside of normal range. The control unit then generates the voltage reference. Voltages references are input to the modulation unit generating the modulation signal for VSC of DVR. The DC link injects or absorbs the required power to compensate the identified voltage sag/swell. Installing an output filter between the VSC and injection transformer reduces harmonic in the output of DVR. Thus, the filter converts the pulse-modulated voltage of the VSC into sinusoidal voltage. The filtered voltage is injected into distribution system via series-injecting transformer. In Fig. 2, PLL represents Phase Log Loop and connection of sensitive load in on the right hand side.
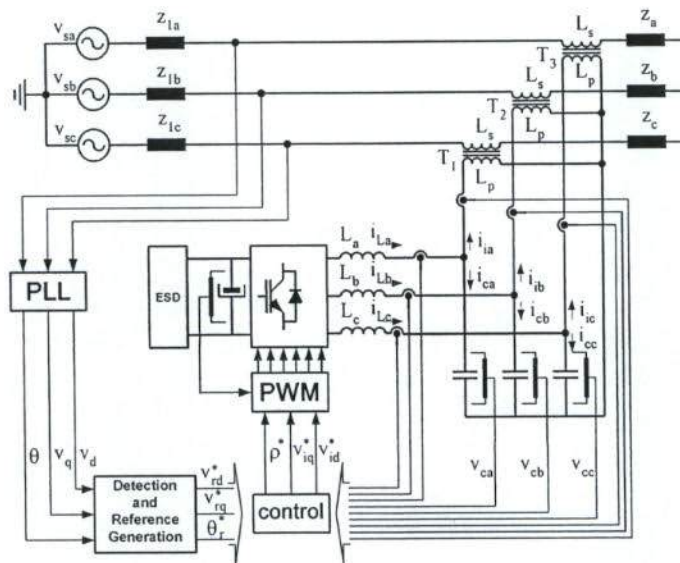

Fig. 2. Schematic diagram of DVR.

3. DVR Control Strategy

A DVR must be able to react very fast on different kinds of voltage sag and swell. The amplitude of the load-side voltage must be restored and for most loads large phase jumps must be avoided. Especially,

the correct compensation of single-phase voltage sag/swell is a major issue. Since DVR uses ESD and DC-link, it will be discharged during the compensation. Hence, the voltage of DC-link will be constantly decreasing during operation mode. Therefore, the modulation index must be kept constant and adapted during the fault. There are two basic control strategies, namely amplitude compensation and amplitude and phase angle compensation adopted for VSC control. In this paper, the later is selected to achieve with optimal control [8]. To avoid a loss of power supply, the amplitude of the load voltage has to be restored by the DVR. The standard solution for compensating voltage sag/swell is to re-establish the exact nominal voltage. Therefore, the amplitude and phase angle of the voltage have to be exactly restored. The resulting vector diagram of DVR compensation for voltage sag/swell as shown in Fig. 3.

The compensation leads to control amplitude and phase angle of load voltage at nominal value. For this strategy, the angle θ of the utility is obtained through the use of a three-phase PLL [11], [12]. As soon as voltage sag/swell occurs, the three-phase PLL will be locked and therefore the phase angle can be restored. Depending on the phase of the new grid voltage, the DVR has to deliver higher voltage amplitude than needed in order to restore the correct voltage magnitude. The system has to be designed for a higher maximum voltage (V_{DVR}) with minimum energy. The required DVR voltage for a sag/swell is given by (1).
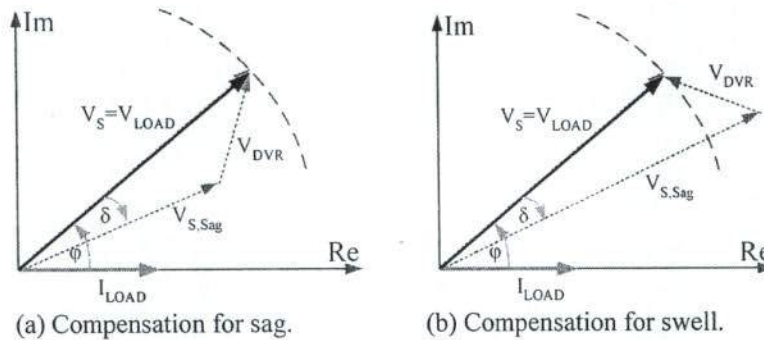

(a) Compensation for sag. (b) Compensation for swell.

Fig. 3. DVR compensation for voltage sag/swell.

$$\hat{V}_{DVR} = \sqrt{\frac{2}{3}} V_N \sqrt{1 + (1-\varepsilon)^2 - 2(1-\varepsilon)\cos\delta} \qquad (1)$$

Where V_N is the nominal grid voltage, ε is sag depth which will be negative for a swell and, δ is the phase depth during the sag and swell period. Fig. 4 shows the curves of different sag/swell and phase jump which is the angle between load voltage and current during the fault.

In order to compensate for the reduced supply voltages to the desired voltage level, the compensation voltage must be injected into the power system by DVR. In this case, the injected compensation voltage must be computed delicately so that the supply voltages may be well-compensated with respect to the amplitude and phase angle of supply voltages.
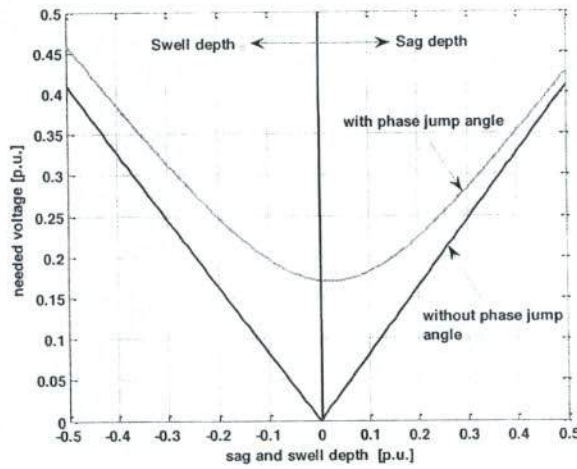
Fig. 4. Voltage amplitude depending on Sag/Swell Depth.

The required active power can be calculated based on the vector diagram. In general, the power must be equal to the difference between load and active power delivered by the grid. The active power equation of DVR is given by (2).

$$P_{DVR} = 3 \cdot (P_{Load} - P_{Grid}) = \sqrt{3} V_N I_N (\cos \varphi - (1 - \varepsilon) \cos(\varphi - \delta)) \qquad (2)$$

Based on (2) the maximum capacitance can be calculated. The active power is limited by the size of DC-link capacitor and the lowest possible DC-link voltage which is sufficient for a proper restoration of the load voltage. Based on these assumptions, the following equation, (3), can be derived for maximum capacitor value.

$$C_{max} = \frac{2 \cdot P_{DVR}}{\left(V_{DC}^2 - \left(\dfrac{\hat{V}_{DVR}}{m_{max} \cdot n} \right) \right)} \times t_{max} \qquad (3)$$

where t_{max} = the maximum compensation time
m_{max} = Maximum modulation index
n = Transformer ratio

4. DVR Mathematical Model

The equivalent circuit of DVR is displayed in Fig. 5, where three-phase voltage of the grid is denoted by v_{sx}. The three-phase voltage and currents of the VSC are denoted by v_{invx}, and i_{Lx}, respectively. The filter capacitor voltages and currents are denoted by v_{cx}, and i_{cx}, respectively. The voltages and current injected by the DVR are denoted by v_{injx}, and i_{injx}, respectively. The DC-link voltage denoted by v_{dc} and the load voltage is denoted by v_{loadx}.
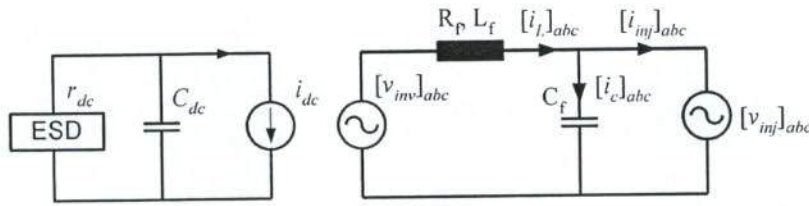
Fig. 5. Single-phase equivalent circuit of grid with DVR.

The control system of the DVR is constituted by two closed-loop controllers connected in cascade: an outer loop that controls the voltage across the filter capacitor $v_{C_fx}(t)$ and an inner controller that controls the current through the filter reactor $i_{L_fx}(t)$. The basic assumption is that the injected voltage is equal to the voltage across the capacitors of the VSC output filter (i.e. the injection transformer is considered ideal with a 1:n turn ratio), $v_{injx}(t) = n \cdot v_{C_fx}(t)$ and $i_{injx}(t) = n \cdot i_{Sx}(t)$, and analogously for the other two phases. Under these assumptions, applying the Kirchhoff's current law (KCL) and Kirchhoff's voltage law (KVL) to the LC-filter, the following differential equations for the three phases can be written

$$i_{L_fx}(t) = i_{C_fx}(t) + i_{injx}(t) = C_f \frac{d}{dt} v_{injx}(t) + i_{injx}(t) \tag{6}$$

$$v_{invx}(t) - v_{injx}(t) - R_f i_{L_fx}(f) - L_f \frac{d}{dt} i_{L_fx}(t) = 0 \tag{7}$$

where x can be replaced with phases a, b and c. By applying Clarke's transformation, (6) and (7) can be written in the αβ-coordinate system as (8) and (9), respectively.

$$\frac{d}{dt} i_{L_f}^{(\alpha\beta)}(t) = \frac{1}{L_f} v_{inv}^{(\alpha\beta)}(t) - \frac{1}{L_f} v_{inj}^{(\alpha\beta)}(t) - \frac{1}{L_f} R_f i_{L_f}^{(\alpha\beta)}(t) \tag{8}$$

$$\frac{d}{dt} v_{inj}^{(\alpha\beta)}(t) = \frac{1}{C_f} i_{L_f}^{(\alpha\beta)}(t) - \frac{1}{C_f} i_{inj}^{(\alpha\beta)}(t) \tag{9}$$

which, by using αβ- to dq-transformation with a PLL synchronized with the grid voltage vector, becomes (10) and (11).

$$\frac{d}{dt} v_{inj}^{(dq)}(t) = \frac{1}{C_f} i_{L_f}^{(dq)}(t) - \frac{1}{C_f} i_{inj}^{(dq)}(t) - j\omega v_{inj}^{(dq)}(t) \tag{10}$$

$$\frac{d}{dt} i_{L_f}^{(dq)}(t) = \frac{1}{L_f} v_{inv}^{(dq)}(t) - \frac{1}{L_f} v_{inj}^{(dq)}(t) - \frac{1}{L_f} R_f i_{L_f}^{(dq)}(t) - j\omega L_f i_{L_f}^{(dq)}(t) \tag{11}$$

with the chosen PLL, the voltage vector is aligned with the direction of the d-axis during steady state. The grid voltage component in the *d*-direction is equal to its *rms*-value (when using power-invariant transformation) and the *q*-component of the grid voltage is equal to zero. Thus, the *d*-component of the current vector (in steady state parallel to the grid voltage vector) becomes the active current component (*d*-current) and the *q*-component of the current vector becomes the reactive current component (*q*-

current). Fig. 6 shows the physical model of DVR with LC-filter. It can be noticed that the coupling terms in the physical model of DVR, the linearity may be deteriorated resulting in an unsatisfactory performance. Therefore, it is necessary to retrieve the linearity of controller so that the control performance, such as fast response and low steady state error, should be enhanced. In conclusion, a vector controller adding the coupling terms as feedforward terms is adopted for driving the DVR.
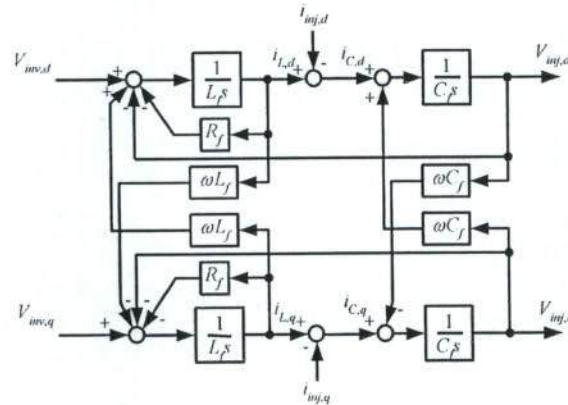

Fig. 6. Physical model of DVR with LC filter.

5. Control Design of DVR

The control technique that has been implemented to control the injected voltage by the DVR is voltage vector control with decoupling approach. To improve the transient response of the DVR and control the injected active and reactive power separately, this control has been implemented in a way similar to the control in speed drives. The ability of voltage sag/swell compensator to effectively protect sensitive loads depends on *the time required by the detection strategy* and *on quality of the injected voltage*. The detection scheme considered in this work uses an algorithm which extracts amplitude, phase and angle information from the utility voltages. The angle θ of the utility is obtained through the use of a three-phase Phase-Locked Loop (PLL). The information extracted from the PLL is used in an algorithm for detection and reference generation, as illustrated in Fig. 7. As it can be seen, the synchronous frame [14], v_d and v_q are used as inputs for low-pass filters to generate voltage references in the synchronous frame.

This information, along with the angle generated by the PLL, is used in the reconstruction of the voltage references in a stationary reference frame. By comparing these voltage references with the instantaneous voltage at the utility grid it is to obtain the command signal for the PWM modulator.
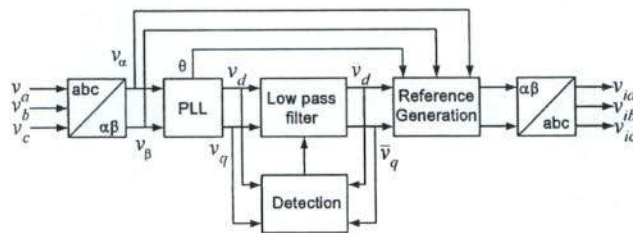

Fig. 7. Detection and reference generation scheme for voltage sag and swell compensation.

From a block diagram of the detection and reference generation scheme as depicted in Fig. 7, the grid voltages (v_a, v_b, v_c) are measured and transformed to a stationary reference frame ($v^{\alpha\beta}$). A PLL is exploited to calculate the transformation angle (θ), which is required to transform the grid voltage from the stationary reference frame to the synchronous reference frame (v^{dq}). Then the grid voltage is subtracted from the reference of the load voltage (v_{load}^{dq}) to calculate the reference of the injected voltage (v_{inj}^{dq*}). The aim of the controller is to keep the load voltage constant. Thus, the DVR should inject the voltage v_{inj}^{dq*} such that

$$v_{inj}^{dq*} = v_{load}^{dq*} - v_s^{dq} \tag{12}$$

where v_{load}^{dq*} is the reference voltage demanded by the load. The missing voltage v_{inj}^{dq*} is injected through the injection transformer. The inputs to the controller are the grid voltages, grid currents, the VSC currents and the capacitor voltages of the output LC-filter. The proposed controller is a discrete controller and uses a sampling time of T_s. Hence the sampling frequency f_s equals to $1/T_s$. The following assumptions are made to derive the controller: 1) the grid current is constant, independent to variations in currents and voltages of the output LC-filter; 2) the capacitor voltage and the inductor current change linearly during one sample period; and 3) the average values of the capacitor voltage and the inductor current are each equal to the half sum of the real value and the reference value at sample k.

To derive the voltage vector controller to be implemented in a digital controller, it is necessary to discretize Eqs. (10) and (11). this is done by integrating the equation over one sample period T_s and then dividing by T_s, thus obtaining

$$\frac{1}{T_s}\left(v_{inj}^{(dq)}(k+1) - v_{inj}^{(dq)}(k)\right) = \frac{1}{C_f}i_{L_f}^{(dq)}(k,k+1) - \frac{1}{C_f}i_{inj}^{(dq)}(k,k+1) - j\omega\frac{1}{C_f}v_{inj}^{(dq)}(k,k+1) \tag{13}$$

$$\frac{1}{T_s}\left(i_{L_f}^{(dq)}(k+1) - i_{L_f}^{(dq)}(k)\right) = \frac{1}{L_f}v_{inv}^{(dq)}(k,k+1) - \frac{1}{L_f}v_{inj}^{(dq)}(k,k+1) - \frac{1}{L_v}R_f i_{L_f}^{(dq)}(k) - j\omega L_f i_{L_f}^{(dq)}(k,k+1) \tag{14}$$

Where $v_{inj}^{(dq)}(k,k+1)$ denoted the average value of $v_{inj}^{(dq)}(t)$ between sample k and sample k+1. Under the assumptions are made in order to formulate the voltage controller [14]. The proportional voltage controller cam now be formulated as (15) and (16).

$$i_{L_f}^{(dq)*}(k) = i_{inj}^{(dq)}(k) + j\frac{\omega C_f}{2}\left(v_{inj}^{(dq)*}(k) + v_{inj}^{(dq)}(k)\right) + \frac{C_f}{T_s}\left(v_{inj}^{(dq)*}(k) - v_{inj}^{(dq)}(k)\right) \tag{15}$$

$$u_{inj}^{(dq)*}(k) = v_{inv}^{(dq)}(k) - \frac{\omega L_f}{2}\left(i_{L_v}^{(dq)}(k) + i_{L_v}^{(dq)*}(k)\right) + \left(\frac{L_v}{T_s} + \frac{R_f}{2}\right)\left(i_{L_f}^{(dq)*}(k) - i_{L_f}^{(dq)}(k)\right) \tag{16}$$

In order to remove static errors due to non linearities, such as noise in the measurements and non-ideal components, an integral part has to be introduced in the control system. The PI-controller can be formulated as

$$i_{L_f}^{(dq)*}(k) = i_{ff}^{(dq)}(k) + k_p \left(v_{inj}^{(dq)*}(k) - v_{inj}^{(dq)}(k) \right) + \Delta i_i^{(dq)}(k) \tag{17}$$

$$u_i^{(dq)*}(k) = u_{ff}^{(dq)}(k) + k_p \left(i_{L_f}^{(dq)*}(k) - i_{L_f}^{(dq)}(k) \right) + \Delta u_i^{(dq)}(k) \tag{18}$$

Where $\Delta i_i^{(dq)}(k)$ and $\Delta u_i^{(dq)}(k)$ are the integral terms for the d- and the q-components, respectively, which can be written as

$$\Delta i_i^{(dq)}(k+1) = \Delta i_i^{(dq)}(k) + k_i \left(v_{inj}^{(dq)*}(k) - v_{inj}^{(dq)}(k) \right) \tag{19}$$

$$\Delta u_i^{(dq)}(k+1) = \Delta u_i^{(dq)}(k) + k_i \left(i_{L_f}^{(dq)*}(k) - i_{L_f}^{(dq)}(k) \right) \tag{20}$$

where the proportional and integral gain of the current and voltage controllers can be written as

Voltage controller gains: $k_p = \dfrac{C_f}{T_s}$; $k_i = k_p \dfrac{T_s}{T_i}$ $\hspace{3cm}$ (21)

Current controller gains: $k_p = \dfrac{L_f}{T_s} + \dfrac{R_f}{2}$; $k_i = k_p \dfrac{T_s}{T_i}$ $\hspace{2.5cm}$ (22)

where T$_i$ is the integrator time constant

Fig. 8 shows the whole control block diagram for calculating the voltage references of inverter. Since the ripple filter current dynamics of (17) must be faster than the compensation voltage dynamics of (18), the controller gain (k_p, k_i) of (17) for faster current dynamics must be determined so that the controller has the time constant of 10 msec. In addition, the controller gain (k_p, k_i) of (18) is determined so that the controller has the time constant of 50 msec.
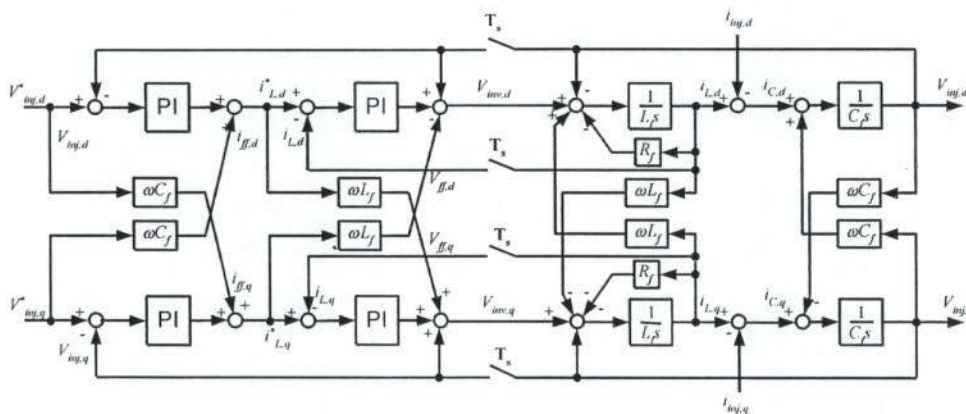

Fig.8. Proposed control strategy of DVR.

6. Simulation Results

To illustrate a typical response of DVR with the proposed control strategy, a simple 50 Hz power distribution system with a sensitive load as shown in Fig. 1 is considered. The system data and parameters are given in Appendix. The performance of DVR with vector control strategy is shown in Fig. 9 for balanced voltage sag due to a three phase fault that was initiated at 0.2 sec. and lasted for 0.05 sec as presented in the supply voltage graph. The load voltage and the injected voltage by DVR are also shown in Fig. 9. As can be seen from the figure, the proposed control strategy is able to drive the DVR to inject the appropriate three phase voltage component with correct phase to remove the supply voltage anomalies due to three phase fault. It was observed that during the normal operation the DVR is not functioning. It quickly injects necessary voltage components to smoothen the load voltage upon detecting voltage sag. Similar performance is observed for an unbalanced voltage sag case as well.

Figure 10 shows the performance of DVR control for unbalanced voltage sag created by double line fault in the system. As depicted in supply voltage the fault was initiated at 0.2 sec and it was cleared at 0.25 sec. As shown in Fig. 10, DVR with the proposed control strategy is quick in injecting the required unbalanced voltage component for correcting the load voltage and keeps it at nominal value.

In order to see the performance of proposed DVR control for voltage swells, a balanced voltage swell was simulated by connecting three phase capacitor banks in the system at about 0.2 sec. The duration of the voltage swell was 0.05 sec. Fig. 11 shows the supply voltage, injected voltage component by DVR and the load voltage. As can be seen from load voltage, the DVR is quick to respond to correct the voltage swell by injecting negative three phase voltage components. Fig. 12 shows the performance of DVR control for unbalanced voltage sag and swell created by single line to ground fault in the system. As depicted in supply voltage the fault was initiated at 0.2 sec and it was cleared at 0.25 sec. As shown in Fig. 12, the DVR with vector control is quick in injecting the required unbalanced voltage components for correcting the load voltage and keep the three phase voltages at nominal values.

In all the cases, the average time taken by the DVR along with the controller to respond for various disturbances is less than 5 μ seconds. However, for other conventional control strategies of DVR, the average response time is found to be more than 10 μ seconds. Table 2 shows the performance of the proposed control compared with the conversional control strategy, both in terms of response time and smoothness of the wave form during voltage sag/swell.

Table 2. Performance of the control strategy.

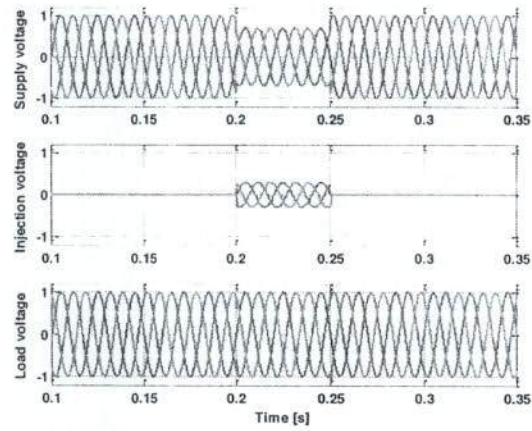| Control strategy	Average Response time	Average THDv
Conversional	> 10 μs	4.31 %
Proposed vector	5 μs	2.47 %

Fig. 9. Response of MV-DVR with vector control for balanced voltage sag.
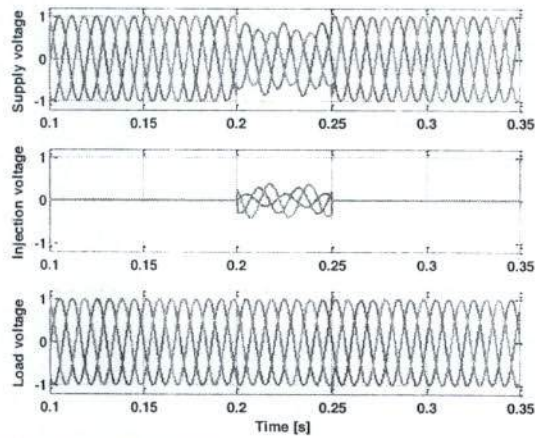
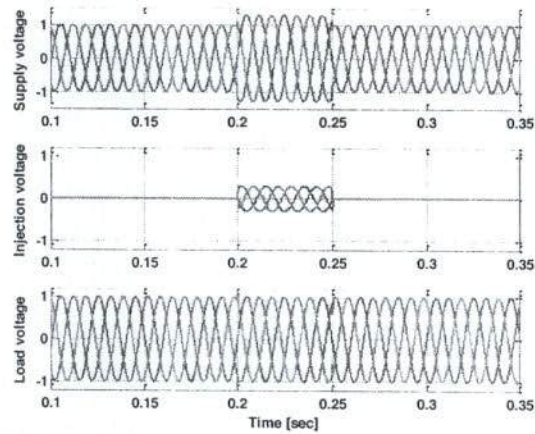Fig. 10. Response of MV-DVR with vector control for balanced voltage sag.

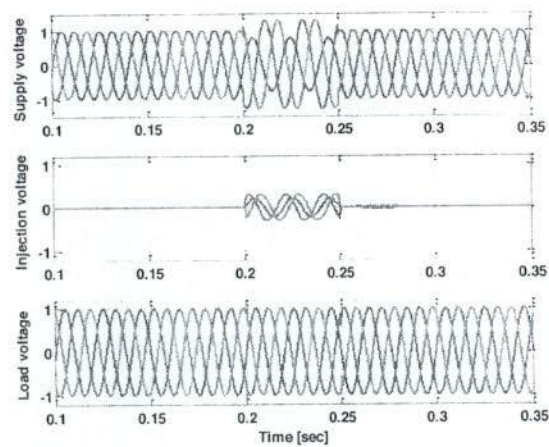Fig. 11 Response of MV-DVR with vector control for balanced voltage swell.

Fig. 12. Response of MV-DVR with vector control for unbalanced voltage swell.

7. Conclusion

A dynamic control strategy has been proposed in this paper for DVR control for mitigating voltage sag/swell. The proposed control strategy known as vector control strategy is widely used in Drives. It is implemented in the synchronous frame with two loops, an inner loop which controls the current and an out loop which controls the voltage. The performance of DVR with vector control has been demonstrated through simulation in a simple distribution system with sensitive load for both balance and unbalanced situations. The proposed control strategy proofs to be performed satisfactory, both in terms of response time and smoothness of the injected voltage components. The response time of the DVR with the proposed control strategy was less than half compared to the same of conventional counterparts.

Acknowledgements

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